Cost and Investment Implications of 3D NAND

Florian Beug, Thomas Melde, Stefan Slesazeck, Gregory Wong



For internal use only

August 2014

This publication is for your internal corporate use only. This document or its contents shall not to be distributed or disclosed to third parties without prior written consent from Forward Insights.



Agenda

- Process Flow Assumptions
- Process Complexity/Process Steps
- Greenfield Investment
- 2D to 3D NAND Conversion
- 32L to 64L 3D NAND Migration



Process Flow Assumptions



For internal use only



Key Features

Key Issues

INSIGHTS

3D NAND Construction Kit





CMOS below array with two finalized metal layer



For internal use only

August 2014

Structure of the p-BiCS concept









Xxxxxxx select gate xxxxxxxxx and removal of the xxxxxxxxxx to allow xxxxxxx of all xxxxxxxx





For internal use only

August 2014





For internal use only

August 2014

xxxxxxxx formation to the xxxxxxxxx to provide xxxxxxxxxxxxxxx to the gate planes and CMOS part



For internal use only

Schematic overview of the fundamental structure of the TCAT concept used in our proposal and the Samsung reference for V-NAND







For internal use only





Finalization of the memory cells by deposition of the xxxxxxxx xxxxxxx, the electrical connection of the xxxxxxxxxxxx is solved by a xxxxxxxxx through the xxxxxxxx creating a rectangular xxxxxxxxxxxxx





The 3D structure after the xxxxxxx and subsequent xxxxxxxxxxxxx finally the xxxxxxx is filled with xxxxxx and polished





The xxxxxxx gate planes and the CMOS devices are contacted in the xxxxxxxxxxxxx by contacts with a xxxxxxxxxxx difference





Comparison of the charge trap layer arrangement in (a) BiCS and (b) TCAT and (c) SMArT





b)



a)

Periphery	Array

I



Vert. FG structure after xxxxxxxxxx removal to open the xxxxxxxxxxxxxxxx deposition and xxxxxxxxxxxxxxxx formation









Vert. FG structure with formed connections to realize xxxxxxxxxxxxxxxxxxxxxxx





Process Complexity/Process Steps



Overview of the key contributors for 16nm NAND process complexity compared to 3D NAND



• Process complexity is at least xx% higher for 3D NAND vs. 2D NAND



Process Complexity Drivers – 32L 3D NAND



• xxxx higher process complexity due to more process steps for xxxxxxxxxx and xxxxxxxxxxxxxxxxx independent of the memory device formation

• CMOS under the array has xx% adder due to xxxxxxxxxxxxxxxxxx layers

```
August 2014
```

For internal use only

Number of process steps by process group – 32L 3D NAND





Process Complexity Drivers – 64L 3D NAND





Number of process steps by process group – 64L 3D NAND



- xxxxxxxxxxx process steps are required for 64L vs. 32L, xxxxxxxx ~xx%
- for example, 32L TCAT/SMArT has xxxx process steps



For internal use only

Lithography Layers by Technology



• shift from xxxxxxxxx to xxxxxxxxxxxx litho steps for xxxxxxxxxxxxxxxxxxxx



Main Thin Film Layers by Technology



• ALD for xxxxxxx formation in 16nm NAND; for xxxxxxxxxxxxxxxxx in 3D NAND



Main Etch Layers by Technology





Main Clean Layers by Technology





3D NAND Tool Commonality with 2D NAND



xxxxx of the total tool types used in 2D NAND and 3D NAND are common



August 2014

2D NAND Tool Re-use in 3D NAND



• xx% of the total tool types used in 2D NAND can be re-used in 3D NAND



Greenfield Investment



Fab Investment by Technology





Number of Equipment



• xx-xx% xxxxxxx required for 3D NAND



Equipment Investment Breakdown by Technology



• xxxxxxxxxx drive xxxxxxxxx investment



For internal use only

Equipment Investment Breakdown by Process Module



etch/cleans + films accounts for over xx% vs. xx% for 2D NAND



For internal use only

August 2014

Equipment Investment Breakdown by Process Module



• xxxxxxxxx investment by process module



Fab Investment by Tool Class



xxxxxxx dominates investment followed by xxxxxxx



For internal use only

Equipment Footprint for 100kwpm Capacity



xx-xx% xxxx space required for 3D NAND



Equipment Footprint Breakdown by Process Module for 100k wpm Capacity



 etch/cleans + films accounts for xx% of footprint in p-BiCS; xxx for other 3D concepts and xx% in 2D NAND



For internal use only

August 2014

Wafer Raw Processing Time Breakdown by Process Module



• etch/cleans + films accounts for xx% in 3D NAND vs. xx% for 2D NAND



For internal use only

August 2014

Wafer Processing Cycle Time by Technology



cycle times are xx-xx% xxxxxxx than 2D NAND



For internal use only

Front End Wafer Cost by Technology



• FE wafer cost is at xx% xxxxxx for 3D NAND



For internal use only

Front End Wafer Cost Breakdown



capital cost accounts for xxxxx of FE wafer cost for 3D NAND



Fab Investment Sensitivity Analysis





For internal use only

2D to 3D NAND Conversion



For internal use only

August 2014

Equipment Footprint Breakdown for Given Area by Process Module for 32 Layer 3D NAND



etch/cleans + films accounts for xxxx xxxxx vs. xx% for 2D NAND



August 2014

Impact on Wafer Capacity of Conversion from 2D NAND to 3D NAND



• xx-xx% wafer capacity xxxxxxx for 3D NAND vs. 2D NAND



For internal use only

Invest/De-invest for Conversion from 2D NAND to 3D NAND



• xxxxxxxxxx results in xxxxxxxxx of ~\$xxxx which must be sold or re-deployed



Breakdown of Tool De-invest



• xxxxxx is due xxxxxxxxxxxxxxxx and can be re-used in 3D NAND production if there is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx available



Incremental Invest by Technology for Conversion from 2D NAND to 3D NAND



• xxx% of the incremental investment for conversion to 3D NAND is in the xxxxxxxx and xxxxxxxx modules



August 2014

De-invest by Technology for Conversion from 2D NAND to 3D NAND





32L to 64L 3D NAND Migration



Impact on Wafer Capacity of Conversion from 32L to 64L 3D NAND



• increasing the number of layers from 32 to 64 results in xxxxxxxxxxxxxxxxxxxxxx of xx% to almost xx%.



Investment/De-investment for Conversion from 32L to 64L 3D NAND





Incremental Investment by Technology for Conversion from 32L to 64L 3D NAND



De-invest by Technology for Conversion from 32L to 64L 3D NAND





Wafer Raw Processing Time Breakdown by Process Module



• Films and Etch/Clean accounts for xx% of the wafer raw processing time for a 64 layer 3D NAND, xxxxxxxxxx xx% for 32 layer 3D NAND



August 2014

Wafer Processing Cycle Time by Technology



fab cycle time is approximately xx% to xx% xxxxxxx for 64 layer
3D NAND compared to 32 layer 3D NAND



Front End Wafer Cost by Technology



• FE wafer cost for 64L 3D NAND xx-xx% xxxxxxx than for 32L 3D NAND



August 2014

Front End Wafer Cost Breakdown



capital cost accounts for xx-xx% of FE wafer cost





Relative Comparison of 2D NAND and 3D NAND

	Relative Comparison of 2D NAND and 3D NAND				
			TCAT/		
	2D NAND	p-BiCS	SMArT	Vert. FG	
Fab Investment					
Cleanroom Space					
Fab Cycle Time					
Wafer Cost					
Surplus Eqt from Tech Migration					
Wafer Capacity / sq. meter					





Market and Technical Intelligence for Semiconductor Memories, Emerging Memory Technologies and Solid State Storage



www.forward-insights.com



For internal use only